CBCS Scheme

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15EC33

# Third Semester B.E. Degree Examination, Dec.2016/Jan.2017
## Digital Electronics

Time: 3 hrs. Max. Marks: 80

**Note: Answer FIVE full questions, choosing one full question from each module.**



### Module-1

1 a. Define the following: i) TVUM Table; ii) Combinational circuit; iii) Cannonical SOP; iv) Cannonical POS. **(04 Marks)**

b. Obtain minimal expression using k-map for the following incompletely specified function: $F(a, b, c, d) = \sum_{m}(0,1,4,6,7,9,15) + \sum_{d}(3,5,11,13)$ and draw the circuit diagram using gates. **(06 Marks)**

c. Write the truth table and design a circuit to generate o/p using K-map for the problem statement given: o/p of a combinational circuit having 4 inputs and an o/p, becomes logical '1' when two or more inputs goto logic level '1'. **(06 Marks)**

**OR**

2 a. Define K-map, incompletely specified function, essential prime implicants and grey code. **(04 Marks)**

b. Obtain minimal logical expression for the given maxterm expression using K-map. $f(a,b,c,d) = \pi_{M}(0,1,4,5,6,7,9,14).\pi_{d}(13,15)$. **(04 Marks)**

c. Use Quine McCluskey's method of minimization to obtain essential prime implicants and minimal expression for the following minterm expression: $f(a, b, c, d) = \sum_{m}(0, 1, 4, 5, 7, 8, 13, 15) + \sum_{d}(2)$. **(08 Marks)**

### Module-2

3 a. Define encoder, decoder, priority encoder and multiplexer. **(04 Marks)**

b. Write block diagram representation of a full adder using 3:8 decoders. **(04 Marks)**

c. Design full adder using i) 8:1 MUX and ii) 4:1 MUX. **(08 Marks)**

**OR**

4 a. Explain Carry look ahead adder with neat diagram and relevant expressions. **(08 Marks)**

b. Design 2-bit comparator and briefly explain. **(08 Marks)**

### Module-3

5 a. Define bistable element, latch, flip-flop and function table. **(04 Marks)**

b. Sketch timing diagrams for JK flipflop and D-flip-flop. **(06 Marks)**

c. Explain M/S JK flip-flop with the help of circuit diagram and waveforms. **(06 Marks)**

**OR**

6 a. Find characteristic equations for T and SR-flip-flops with the help of function tables. **(06 Marks)**

b. Write circuit diagram for the edge triggered D-flip-flop and provide explanation for different input condition. **(06 Marks)**

c. Explain the operation of a switch debouncer built using SR-latch with the help of waveforms. **(04 Marks)**

## Module-4

7 a. Define register, asynchronous ripple counter synchronous counter and ring counter. **(04 Marks)**

b. Design mod-8 counter using right shift register. Use D-flip-flop to build register circuit. Explain the operation using function table. **(06 Marks)**

c. Write timing diagrams, counting sequence and the logic diagram for 4-bit ripple counter and briefly explain. **(06 Marks)**

**OR**

8 a. Explain PIPO and SIPO operations using single diagram. **(06 Marks)**

b. Design Mod-6 synchronous counter using JK flip-flop. The sequence is 000, 001, 011, 100, 101, 111...000. **(07 Marks)**

c. Write state diagram for Mod-5 self correcting counter and briefly explain. The sequence is 000, 001, 101, 110, 111, 000. **(03 Marks)**

## Module-5

9 a. What are Melay and Moore models of a sequential circuit? Briefly explain with diagrams. **(04 Marks)**

b. Write characteristic/excitation table for JK flip-flop and explain. **(03 Marks)**

c. Analyze the following sequential circuit. Writ excitation equations K-maps and state diagrams to analyze. **(09 Marks)**

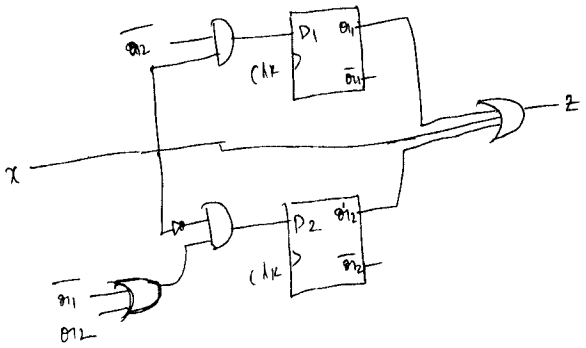


Fig.Q.9(c)

**OR**

10 a. Write state diagrams for a four state machine using Melay and Moore models and briefly explain. **(04 Marks)**

b. What is a state table? Give an example. **(02 Marks)**

c. Design a counter circuit for the following state table. Follow the standard steps for design. **(10 Marks)**

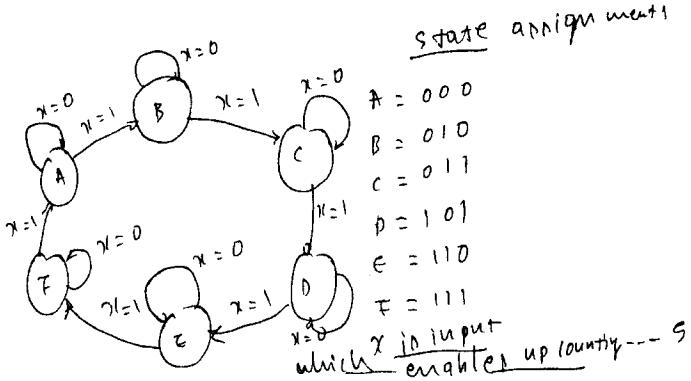


Fig.Q.10(c)

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